PH-7 (C4-P02)
Core Board Specifications And User Manual

LPWA&LTE Standard Module Series

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Document History

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Catalog

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1 Core Board Introduction

The PH-7 core board adopts 2.54mm pin design and provides 38-pin pins, including function pins and enable control pins. The main pins provide support and convenience for customers to develop, debug, and mass produce equipment.

Design concept: PH-7 is neutral, and water is the most common neutral substance, which is widespread, close to life, and indispensable; secondly, it also means that users should guard against arrogance and impatience, and their mentality should be as soft as water.

The core board supports Python and Open secondary development. This manual mainly introduces the Python version.

Python development materials summary:

https://python.quectel.com/download

Python development API documentation:

https://python.quectel.com/doc/API_reference/zh/index.html

1.1.Applicable Core Board And PN

The core boards and update module models applicable to this manual are as follows:

Table 1：Applicable core board

PN	Description
BG&EG series core board	Pin-type core board, leading out common and key pins

Table 2：Applicable module models

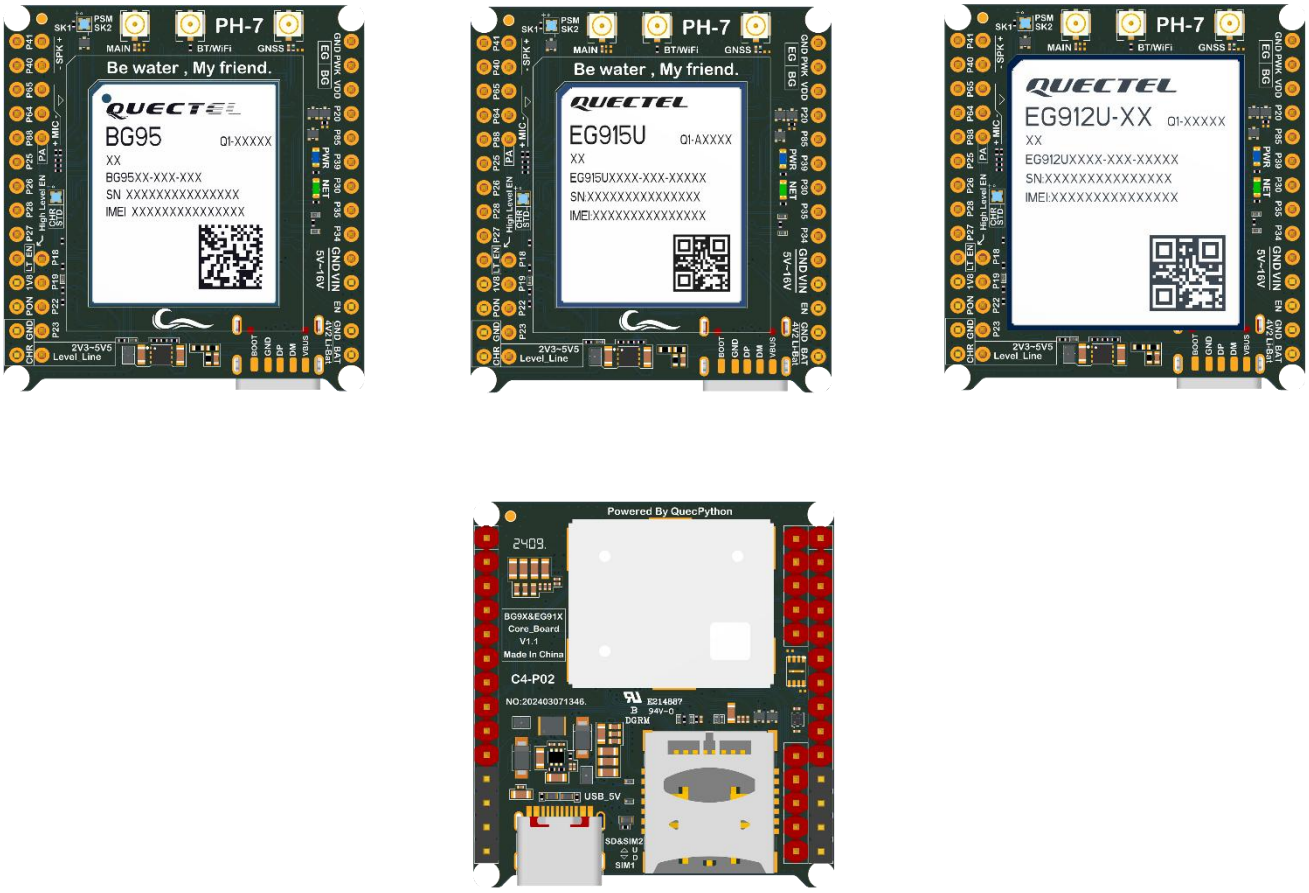
PN	Description
BG&EG series core board	Applicable to BG95, BG96 full series, EG915UEUAB, EG915ULAAB, EG912UGLAA and other EG series, including, but not limited to the above module models. Some functional application adaptation may be lacking, please refer to the QuecPython official website Python development API documentation for details.

1.2 Characteristic

- Complete function coverage
- Compatible with many module models
- Compatible with different voltage levels
- Pin interface for easy external debugging

- Support common function interfaces such as GPIO/UART/IIC/SPI/USB
- Support lithium battery charging function
- EG series supports analog audio input and output
- Support Python secondary development or Open C development

2 Core Board Rendering



(The above pictures are for reference only, please refer to the actual product)

Picture 1：PH-7(C4-P02)Core board rendering

3 Specification

This chapter mainly summarizes the specific specifications of the PH-7 core board and some device precautions.

Tanle 3：Specification

	Entry	Description
Electrical parameters	Temperature	Operating temperature: -35 ~ 75℃ (see note 1 below) Extended temperature: -40 ~ 85℃ (see note 2 below)
	Operating Humidity	Unknown, according to actual situation.
	Power supply interface	2.54mm pin, Type-C (USB2.0/USB3.0)
	Supply voltage	Normal working voltage range of USB power supply: ≤5.1V:3A; ≥5V:2A External pin power supply range: ≤16V:3A; ≥5V:2A BAT battery power supply: 3.7V rechargeable lithium battery
RF Performance	Frequency band	For details, refer to the module specification
		For details, refer to the module specification
	Transmit power	For details, refer to the module specification
		For details, refer to the module specification
UART	Interface Type	Contains function reuse, please refer to the reuse table for details. Connection method: pin (2.54mm)
SPI	Interface Type	Contains function reuse, connection method: pin (2.54mm)
IIC	Interface Type	Contains function reuse. Connection method: pin (2.54mm)
USB*1	USB Interface	Type-C female port，Supports power supply and software debugging, as well as burning firmware and updating Python scripts
LED*7	PWR	Power indicator, ice blue, always on after power on
	NET	The default is the module network status indicator. Connect the module P21 pin
	SK1	Onboard SIM1 card slot indicator: When SIM card 1 is inserted and recognized normally, the indicator light stays on; when SIM card 1 is removed, the indicator light goes off.

	SK2	Onboard SIM2 card slot indicator, when SIM2 is inserted and recognized normally, it stays on, and when SIM2 is removed, it goes out. (Only supports EG dual-card series, requires firmware support.)
	PSM	The light stays on when the module turns on PSM or enters PSM state.
	CHR	Blue, long light during charging
	STD	Emerald green, bright when full
ADC	Interface Type	ADC0 is connected to VBAT by default, satisfying VBAT:ADC0=4:1
GPIO	Interface Type	Including multiplexed GPIO, see the function reuse table for details, 2.54mm pin external
Level_Line	Level Line	2.3V-5.5V, level adaptive, used for level conversion IC host side level, if the default level is 3.3V, it can be left unconnected
PWM	Interface Type	With function reuse, 2.54mm pin external connection
LT_EN	Level Enable	High level is effective
PON	PSM wake-up	PSM_EINT pin, can wake up the module from PSM
MIC&SPK	Analog Audio	Analog audio interface
PA	PA Enable	Pull high to enable SPK PA output

Table 4： Automatic startup And BOOT

Automatic startup	EG	EG series short pin automatic start
	BG	BG series short pin automatic start
BOOT	USB_BOOT	Lead out as a test point

Remark

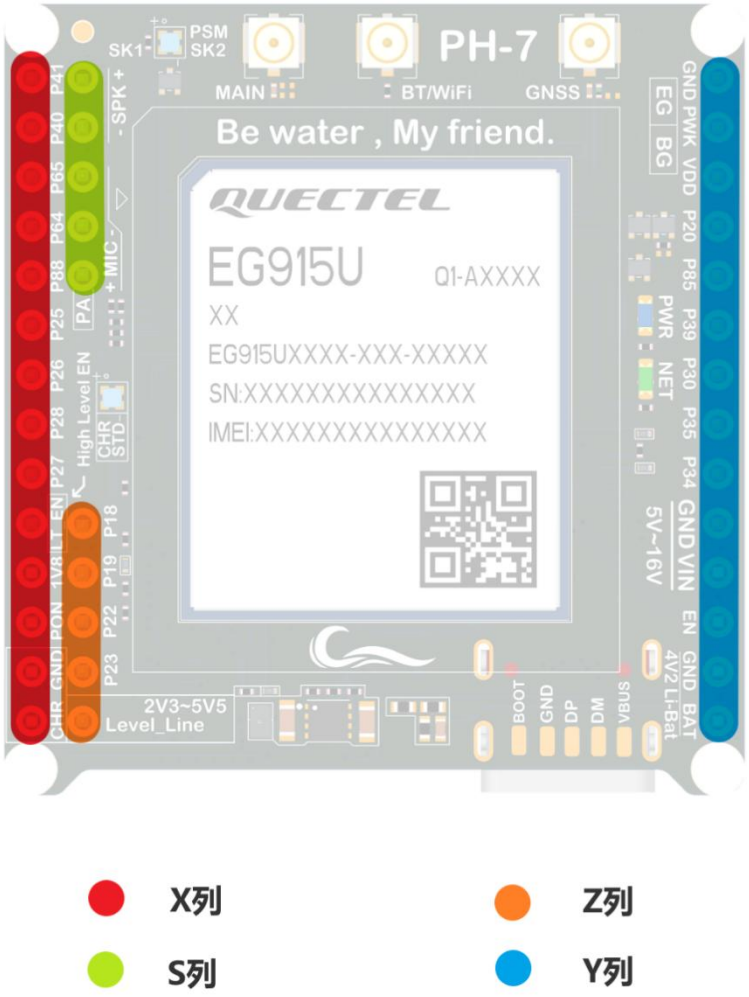
1.Within this working range, the performance of the equipment meets the requirements of the 3GPP standard.
2.Within this working range, the radio frequency and network are basically not affected, and only a few indicators exceed the 3GPP standard. When the operating temperature is restored, all indicators still meet the 3GPP standard.

4 Pin specification

This section introduces the pins of the PH-7 core board. The functions are described as follows:

4.1.Pin Correspondence Diagram

The following figure takes the EG915U core board as an example:



Picture 2：Schematic diagram of the core board pin correspondence

表 5：核心板引脚功能复用表

GPIO14		BG_CS1		BG&EG_SDA1	**P41**	X1	S1	**SPK_N**	Y1	**GND**					
GPIO13		BG_CLK1		BG&EG_SCL1	**P40**	X2	S2	**SPK_P**	Y2	**POWERKEY**					
BG_GPIO16	BG_RX2	BG_MISO1			**P65**	X3	S3	**MIC_N**	Y3	**VDD_EXT**					
GPIO15	BG_TX2	BG_MOSI1		EG_MOSI0	**P64**	X4	S4	**MIC_P**	Y4	**P20**			EG_PWM0	BG_GPIO22	EG_GPIO16
GPIO21				EG_MISO0	**P88**	X5	S5	**PA**	Y5	**P85**		BG_PWM1		BG_GPIO18	EG_GPIO18
GPIO9		BG_SDA2	BG_CS0	EG_CS0	**P25**	X6			Y6	**P39**	RI			BG_GPIO30	EG_GPIO25
GPIO10		BG_SCL2	BG_CLK0	EG_CLK0	**P26**	X7			Y7	**P30**	DTR			BG_GPIO24	EG_GPIO20
GPIO12	BG&EG_RX1		BG_MISO0		**P28**	X8			Y8	**P35**	TX	BG_UART4	EG_UART2	BG_GPIO26	
GPIO11	BG&EG_TX1		BG_MOSI0		**P27**	X9			Y9	**P34**	RX			BG_GPIO25	
					LT_EN	X10	Z1	**P18**	Y10	**GND**					
					1V8	X11	Z2	**P19**	Y11	**VIN**					
					PON	X12	Z3	**P22**	Y12	**EN**					
					GND	X13	Z4	**P23**	Y13	**GND**					
					CHRG	X14	Z5	**Level_Line**	Y14	**BAT**					
							Z1			BG_SCL0		BG_CLK2	EG_RX4	BG_GPIO5	EG_GPIO5
							Z2			BG_SDA0		BG_CS2	EG_TX4	BG_GPIO6	EG_GPIO6
							Z3	DBG_RX		BG_RX0		BG_MISO2		BG_GPIO7	
							Z4	DBG_TX		BG_TX0		BG_MOSI2		BG_GPIO8	

备注

BG:suitable for BG9X module

EG:suitable for EG91X module

：Basic serial port function pins, AT standard firmware can be used

*The above table does not represent the pin functions of the entire series. Please compare according to the specific model used.

4.2 Function Description

To help users quickly get started with the core board, this section briefly introduces how to use the core board functions and precautions.

4.2.1 Charging And USB

When the Type-C interface is plugged in to connect the USB, the charging function is enabled by default and cannot be turned off. If you do not use the charging function, ignore it.

If you use an external power supply to charge, please connect the power ground and the positive pole of the 5V-16V power supply to the X13 X14 pins to charge the battery mounted on the Y13 Y14 pins. (The battery must be mounted with a 4.2V rechargeable battery)

It is not recommended to charge while using USB and connecting CHRG (X14 pin).

4.2.2 Power Enable

The core board is enabled by default when powered on. If you need to power off the core board during the use of the whole device.

1. Directly disconnect the VIN power supply externally

1、 2. Pull down the EN (Y12) pin to turn off the DCDC output. (See Note 1 below)

4.2.3 Level conversion

The core board has an onboard 3.3V level conversion IC. To reduce power consumption, the level conversion is disabled by default. During use, please pull up the LT_EN (Y10) pin externally, or use a jumper cap to short-circuit the two adjacent pins LT_EN (Y10) and 1V8 (Y11) to enable level conversion.

4.2.4.GNSS

The GNSS function depends on the module model. Taking BG95 as an example, the core board uses an active antenna by default, and the power supply to the active antenna is turned on by default.

1. AT standard firmware, use AT+QPGS=1 to turn on the GNSS function. No need to control active power supply.

2. Secondary development firmware, since the initial pin level is uncertain, if you need to turn on the GNSS active power supply, please pull down the module P37 pin. Pull up the P37 pin to turn off the GNSS active power supply.

4.2.5.SD And DualSIM Card

Taking EG912UGLAA as an example, if you need to use the SD storage function, after inserting the SD card, please pull up the P36 pin to enable power supply to the SD, and then use the SD function. Since the positions of SIM2 and SD card overlap, if the firmware supports SIM2, SIM2 and SD cannot be used at the same time.

4.2.6.Flash（Optional）

The onboard Flash is not mounted by default. If you need to use Flash, please contact us separately.

4.2.7 Analog Audio

The core board has MIC circuit and SPK&PA amplifier circuit on board. Here we take EG912UGLAA as an example.

1. When using AT standard firmware, if you need to play audio externally, please pull up the PA (S5) pin to enable PA

2. When using Python firmware, pull up PA (S5) externally or pull up the P114 pin in the module program (see Note 2 below)

4.2.8.ADC

The core board has an onboard ADC for developers to use. ADC0 is connected to VBAT by default, satisfying VBAT:ADC0=4:1

4.2.9 Low power consumption

For module models that support PSM, the core board power consumption can be reduced to an extremely low level. For specific implementation, please refer to the module specification or QuecPython official website.

4.2.10 PSM and wakeup

For module models that support PSM, the core board can externally wake up the module that enters PSM low power consumption.

1. Pull down POWERKEY.

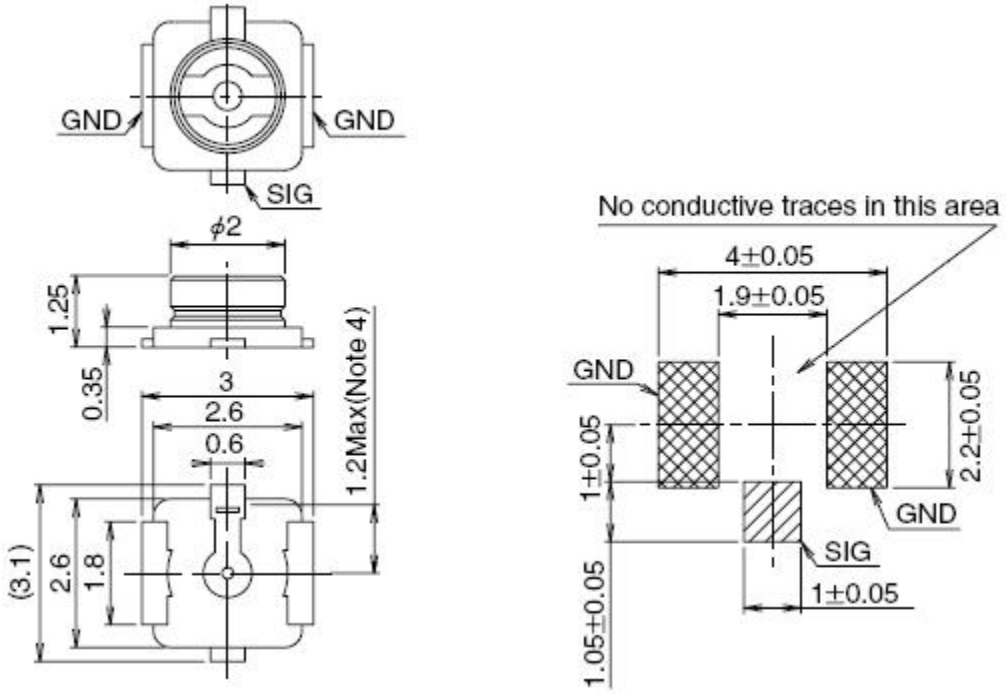
1、 2. Pull up the PON (X12) pin, or short-circuit the adjacent pins X12 and X11. (See Note 3 below)

Remark

1. EN high level depends on VIN voltage, for example: if VIN is 12V, then EN level is 12V. If you use external pull-down EN, please use MOS tube control, and do not directly connect IO of different levels for control.
2. Since PA pin is directly connected to module pin, the level is 1.8V. When external pull-up, please connect to Y11 or X3 pin of core board.
3. Since PON is directly connected to module pin, the level is 1.8V. When external pull-up, connect directly short-circuit X12 X11 pin of core board.

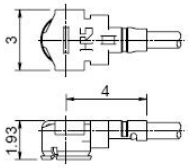
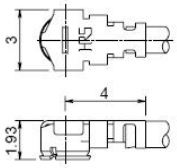
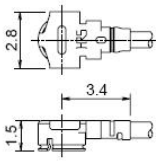
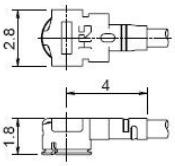
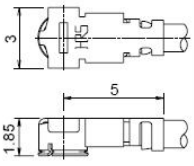
5 Antenna interface

The core board is equipped with a RF connector (socket) for easy antenna connection. The dimensions of the antenna connector are shown in the figure below.



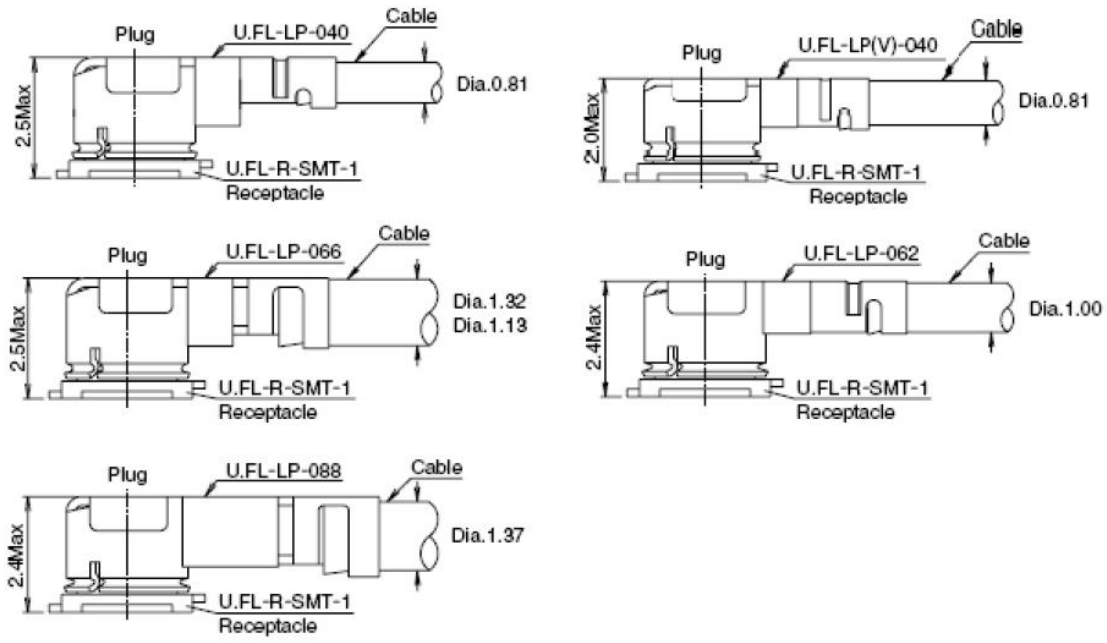
Picture 3：Antenna connector size（Unit：mm）

The U.FL-LP series cables listed in the figure below can be used with the antenna connector.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Picture 4：U.FL-LP Connection line series

The following figure shows the installation dimensions of the connecting wire and connector：



Picture 5：Installation Dimensions（Unit：mm）

6 Reliability And Electrical Performance

This chapter mainly introduces the electrical characteristics of the core board interface, including：

- Power characteristics
- Electrostatic protection

6.1 Power characteristics

The USB input voltage of the core board is 5.0~5.1 V, and the pin input voltage is 5V-16V, which is then converted to 3.8V by DCDC to supply the module. The power requirements are shown in the following table：

Table 6：Input Range

Parameter	Description	Minimum	Typical Value	Maximum	Unit
VBUS	USB Supply Power	5	5.0	6	V
VIN	Outer Supply Power	5	5.0	16	V

Table 7：I/O Requirement

Parameter	Description	Minimum Value	Maximum Value	Unit
VIH	Input high level	0.7 × VCC	VCC + 0.3	V
VIL	Input low level	-0.3	0.3 × VCC	V
VOH	Output high level	VCC - 0.5	VCC	V
VOL	Output low level	0	0.4	V

*Note: VCC typical value is 3.3V

6.2 Electrostatic Protection

Since static electricity generated by human body static electricity, charged friction between microelectronics, etc. will be discharged to the module through various channels and may cause certain damage to the module, it is necessary to pay attention to static electricity protection and take reasonable static electricity protection measures. For example: wear anti-static gloves during R&D, production, assembly and testing; when designing products, add anti-static protection devices at circuit interfaces and other points susceptible to electrostatic discharge.
The following table shows the ESD withstand voltage of the module pins.

Table 8：The module's own electrostatic protection value is as follows：

Test interface	Contact discharge	Air discharge	Unit
Power and ground interface	±4000	±8000	V
Antenna interface	±4000	±8000	V
Other interfaces	±500	±1000	V

7 Precautions

Please pay attention to the following when using the core board.

7.1 Spraying

If you need to spray the core board, please ensure that the spray material used does not chemically react with the module shield or PCB, and ensure that the spray material does not flow into the module.

7.2 Cleaning

Do not perform ultrasonic cleaning on the communication module mounted on the core board, otherwise the crystal inside the module may be damaged.

7.3 Booting

Short-circuit the BG or EG automatic power-on pin to enable the module to automatically power on. If power on and off needs to be controlled, the POWERKEY pin can be connected to an external control circuit.

Remark

This manual does not represent any position or opinion of Quectel. Any losses caused by incorrect operation according to the guidance of this manual have nothing to do with Quectel module products.

8 Appendix

Table 10：Reference Document

Document Name
[1] Quectel _EVB_User Instruction
[2] Quectel_LTE Standard(A)_Series_AT_Commands_Manual